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PHASE ERROR DETECTOR USING I/Q INTERFERENCE CANCELLATION

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FIELD OF THE INVENTION:

The present invention relates to estimating and correcting phase error of a received signal wherein an in-phase portion and a quadrature portion of the received signal are independently spread or scaled.

BACKGROUND:

In a spread spectrum communication system, symbols or packets are spread and scrambled prior to transmission. While the spreading code used to spread an in-phase (I) component of the transmitted signal $s(t)$ may sometimes be identical to that used for the quadrature (Q) component, generally the scrambling codes differ. The end result is that the I and Q components are identified by different component spreading codes c_I and c_Q. A receiver generally acquires at least the initial spreading codes from one or more synchronization channels, which also provide the receiver with phase/frequency to be used for demodulating the received signal $r(t)$. However, the signal is subject to phase errors introduced in the transmission channel that are not accounted for by information provided over the synchronization channel.

Bi-BPSK is a modulation technique wherein each of the in-phase (I) and quadrature (Q) components of a received signal $r(t)$ are treated as independent binary phase shift keyed (BPSK) signals. In general, each of the two BPSK signal components may be independently scaled and/or spread, generally using different component spreading codes c_I and c_Q or scaling factors. Though the data rates over the I and Q channels may differ at any given instant, the chip rate of each (the rate of the spreading sequences in a spread spectrum communication) is generally identical.

A Bi-BPSK constellation is shown in Figure 1, wherein the constellation points are located at positions (-2, -1), (-2, 1), (2, -1) and (2, 1), and received points are grouped about the true constellation points. Where the I axis is horizontal representing a cosine function and the Q axis is vertical representing a sine function, phase error introduced in a transmission channel tends to

rotate the vector defining the point relative to the I and Q axes. Phase error correction seeks to drive the I or Q value to zero by de-rotating the position vector of received points. This clusters received points more tightly about the actual constellation points, reducing error in resolving which of the constellation points the received point truly represents. Correcting for phase error

5   clusters all of the received points more closely toward the constellation points, eliminating ambiguities that may be otherwise cause a received point to be wrongly decided. In the prior art, phase error correction is typically done on the Q channel, since it generally represents the stronger signal, provided the Q channel is spread more. To derotate the phase error, the prior art used a closed loop to drive the product of $IdQ*sign(QdQ)$. Bi-BPSK often takes the approach of using a

10   single carrier phase error term to resolve phase error in both the I and Q channels. That prior art approach is subject to higher phase jitter in the carrier loop when phase error varies over time, leading to unacceptably high symbol error rates in certain cases. The present invention includes a method and apparatus for reducing phase jitter in the carrier loop and for reducing the commensurate symbol error rate.

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SUMMARY OF THE INVENTION:

The present invention is directed to determining an estimate of phase error in the instance of two orthogonal signal components each spread by a separate component spreading code. Where each signal component is spread by an identical spreading code but scrambled by different scrambling

20   codes, the present invention considers they are spread by separate component spreading codes. The invention includes a method for estimating a phase error, and a phase error detector or estimator that may be a component within a receiver. The estimate of phase error is preferably output to a feedback loop, which the receiver uses to correct phase of subsequently received signals.

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The method includes inputting a first signal component spread by a first spreading code and an orthogonal second signal component spread by a second spreading code. What is termed herein as a cross-despread value is determined by despreading the first signal component with the second spreading code. An estimate of interference from the second signal component into the first

2

signal component is then calculated, and the estimate of phase error is determined by subtracting the estimate of interference from the cross-despread value. Preferably, the above is done in parallel for each of the first and second signal components, each result is scaled by a factor to maximize a signal to noise ratio, and the results are combined to yield an estimate of phase error

5   that is accurate at least in the range of small phase errors, and that reduces jitter in the carrier loop as compared to other methods. Details are provided below.

A phase error detector according to the present invention includes first and second despreaders, a discriminator, a multiplier, and an adder. The detector has a first input for receiving a first signal

10   component that is spread with a first component spreading code. The first despreader despreads the first signal component with a second component spreading code associated with a second signal component, where the second signal component is orthogonal to the first. The second despreader is in parallel with the first, and depsreads the first signal component with the first component spreading code. The discriminator has an input coupled to an output of the second

15   despreader, and outputs a data symbol estimate of the first signal component. The multiplier takes an estimate of interference from despreading the first signal component with the second spreading code, and multiplies it by the data symbol estimate. In the example given, the estimate of the data symbol is selected from the set {-1, +1}, so the multiplier serves to determine the sign (+ or -) of the estimate of interference. The adder takes inputs from the multiplier and the first

20   despreader, and subtracts the interference estimate from the first signal as despread by the second component spreading code.

Preferably, the phase error detector includes duplicates of the above components to process each of the first and second signal components as above in parallel, and then combines the two results

25   after scaling to output a phase error estimate that exhibits less jitter than prior art approaches. Various details of the preferred and alternative embodiments are described below.

3

BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 is a diagram of a Bi-BPSK constellation with four points, each surrounded by a cluster of received bits.

Figure 2 is a block diagram of a receiver in which phase errors are estimated according to the present invention.

Figure 3 is a schematic illustrating different data rates on the I and Q channels that the preferred embodiment of the present invention resolves.

Figure 4 is a block diagram showing details of the phase error detector of Figure 2 in accordance with the preferred embodiment of the present invention.

Figure 5 is a graph showing phase error detector output versus true phase angle error for four phase detectors: two according to the present invention, one according to a co-pending invention, and one according to the prior art.

Figure 6 is a graph showing variance of detector output versus true phase angle error of the four detectors of Figure 5.

DETAILED DESCRIPTION:

The present invention includes a method and apparatus for estimating phase error for independently spread and scaled in-phase and quadrature Bi-BPSK signals. It is known to despread a received I signal by the Q channel's pseudo-random number (pn) sequence (also known as the Q component spreading code c_Q) to estimate phase error. The present invention significantly improves the performance of that prior art approach by subtracting out an estimate of the interference caused by despreading the I data by the Q pn code (or vice versa). The present

4

invention further improves over the prior art in that it combines two terms, I despread with Q and Q despread with I, from which interference has been subtracted from each, and combines them to achieve a more stable estimate of phase error. This approach improves performance as compared to the prior art, and experimental verification of the improvement is quantified at Figures 6-7. An underlying assumption in the mathematical analysis below is that the chip rates are identical on both the I and Q channels, though the data rates may and typically do differ. In a spread spectrum system, each pulse in the spreading sequence is termed a chip, and the rate of the sequence of pulses is the chip rate.

Mathematically, the transmitted signal may be expressed in complex baseband notation as:

$$s(t) = \alpha_I b_I(t) c_I(t) + j\alpha_Q b_Q(t) c_Q(t) \qquad [1]$$

where α_I and α_Q are the independent scaling amounts for I and Q respectively. The terms $b_I(t)$ and $b_Q(t)$ denote the data symbols, and $c_I(t)$ and $c_Q(t)$ are the independent spreading sequences for I and Q respectively. For Bi-BPSK signals, samples of $b_I(t)$ and $b_Q(t)$ are from the set $\{-1,+1\}$.

Figure 1 shows a prior art signal constellation for the case of $\alpha_I = 1$ and $\alpha_Q = 2$, corresponding to 6 dB more power on I than on Q at the chip level. The constellation points lie at (-2, -1), (-2, 1), (2, -1), and (2, 1) are the constellation points transmitted. The plurality of points clustered about each constellation point represent samples of the received signal for the case of an overall signal to noise ratio of 10 dB.

Assume that a received signal r(t) is a scaled, phase-rotated version of the transmitted signal s(t) with complex additive noise, $n_c = n_I + jn_Q$. This is shown in block diagram form at Figure 2, wherein a transmitted signal s(t) 20 is corrupted with noise 22 and phase error 24 prior to processing at a receiver 26. The received signal r(t) is demodulated, converted to digital, and

input into a digital phase shifter 28 that applies an estimate of the phase error $\hat{\theta}_e$ (30) to the I and Q components. The estimate of the phase error $\hat{\theta}_e$ is calculated in the phase error detector 32 and fed back through a carrier loop 34, preferably after attenuation by a low pass filter 36. In this case, the received signal $r(t)$ may be expressed as follows:

$$r = \beta s e^{j\theta} + n_c = \beta[\alpha_I b_I c_I + j\alpha_Q b_Q c_Q][\cos\theta + j\sin\theta] + [n_I + jn_Q]$$
$$= \beta[\alpha_I b_I c_I \cos\theta - \alpha_Q b_Q c_Q \sin\theta] + j\beta[\alpha_Q b_Q c_Q \cos\theta + \alpha_I b_I c_I \sin\theta] + [n_I + jn_Q] \qquad [2]$$
$$= r_I + jr_Q$$

where

$$r_I = \beta[\alpha_I b_I c_I \cos\theta - \alpha_Q b_Q c_Q \sin\theta] + n_I,$$
$$r_Q = \beta[\alpha_Q b_Q c_Q \cos\theta + \alpha_I b_I c_I \sin\theta] + n_Q. \qquad [3]$$

For brevity, time dependence (t) is not shown explicitly with the variables to which it applies (r, s, b, and c above), but that time dependence remains implicit within the assorted variable names in the equations above and in the following description.

It has been noted that both the I and Q channels are at the same chip rate, but may carry different data rates. Figure 3 illustrates the dilemma, wherein the I channel is running at eight times the rate of the Q channel. The present invention despreads one channel with the spreading code of the other, calculates an interference caused by despreading in that manner, and subtracts that interference from the cross-despread value to determine an estimate of phase error. In a preferred embodiment, this interference cancellation is performed on both channels, and the interference-free estimates are weighted and combined to reduce jitter. However, they cannot be directly combined due to the different data rates. As such, a common rate is found by, in the case of Figure 3, virtually parsing the Q channel into intervals that correspond with the frames of the I channel. This aspect is described more completely below in the description of Figure 4.

The phase error detector 32 is shown in detail at Figure 4. Each of the input signal components r_I

and r_Q are input into the phase error detector 32 and split into two streams. Both signal components are preferably processed in like fashion in parallel. For r_I, a first stream is despread with a first spreading code 38 that is associated with the I component and designated $c_I(k)$; and a second stream is despread with a second spreading code 40 that is associated with the opposing Q

5   component and designated $c_Q(k)$. While only one multiplier 42 is depicted in Figure 4 for each of the streams, in practice the preferred embodiment would impose one multiplier 42 for each of the various k spreading codes used to despread the signal, where k is an integer greater than one. In the embodiment of Figure 4, the multipliers 42 having r(k) and c(k) as inputs operate as sign inverters only.

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Along the first stream associated with the I component of the received signal r_I, the despread

signals $r_I c_I$ are combined at a first I summing block 44A (that operates to perform $\sum\limits_{n=1}^{P_I} r_I c_I$) for all

of the P_I chips per symbol, since the first spreading code $c_I(k)$ 38 was used for the despreading. The output of the first I summing block 44A is the despread value IdI (the I signal component

15   despread with the spreading code associated at the transmitter with the I signal component), detailed below at equation [4]. Along the second stream associated with the I component of the received signal r_I, the despread signal $r_I c_Q$ is combined at a second I summing block 44B (that

operates to perform $\sum\limits_{n=1}^{P_Q} r_I c_Q$) for all of the P_Q chips per symbol, since the second spreading code

c_Q (40) was used for the despreading. As noted in conjunction with Figure 3, the chip rate is the

20   same for both the I and Q channels though the data rate, and hence the processing gains, may differ. The output of the second I summing block 44B is termed the cross-despread value IdQ (the I signal component despread with the spreading code associated at the transmitter with the Q signal component), detailed below at equation [5].

25   In a preferred embodiment, the Q component of the received signal is similarly processed. For r_Q, a first stream is despread with the second spreading code 40 associated with the Q component and designated $c_Q(k)$, and a second stream is despread with the first spreading code 38 associated with the opposing I component and designated $c_I(k)$. Along a first stream associated with the Q

component of the received signal r_Q, the despread signal $r_Q c_Q$ is combined at a first Q summing block 44C (that operates to perform $\sum_{n=1}^{P_Q} r_Q c_Q$) for all of the P_Q chips per symbol. The output of the first Q summing block 44C is the despread value QdQ, detailed below at equation [7]. Along the second stream associated with the Q component of the received signal r_Q, the despread signal $r_Q c_I$ is combined at a second Q summing block 44D for all of the P_I chips per symbol. As with the I streams, the processing gains may differ between the first and second Q streams due to the different spreading codes. The second Q summing block 44D (that operates to perform $\sum_{n=1}^{P_I} r_Q c_I$) outputs the cross-despread value QdI, detailed below at equation [6].

Substituting equations [3] yields the possible despread values, namely,

$$IdI = \sum_{k=1}^{P_I} r_I c_I = \beta \alpha_I b_I P_I \cos\theta - \sum_{k=1}^{P_I} [\beta \alpha_Q b_Q c_Q c_I \sin\theta + n_I c_I] \qquad [4]$$

$$IdQ = \sum_{k=1}^{P_Q} r_I c_Q = \sum_{k=1}^{P_Q} [\beta \alpha_I b_I c_I c_Q \cos\theta + n_I c_Q] - \beta \alpha_Q b_Q P_Q \sin\theta \qquad [5]$$

$$QdI = \sum_{k=1}^{P_I} r_Q c_I = \sum_{k=1}^{P_I} [\beta \alpha_Q b_Q c_Q c_I \cos\theta + n_Q c_I] + \beta \alpha_I b_I P_I \sin\theta \qquad [6]$$

$$QdQ = \sum_{k=1}^{P_Q} r_I c_Q = \beta \alpha_Q b_Q P_Q \cos\theta + \sum_{k=1}^{P_Q} [\beta \alpha_I b_I c_I c_Q \sin\theta + n_Q c_Q]. \qquad [7]$$

Each of the above despread values are bit weighted by the scaling amount α and the processing gain P for the noted I or Q channels. For clarity, the terms IdQ and QdI are referred to as cross-despread values since they include cross-correlation terms due to despreading with the codes associated with the orthogonally opposed signal component.

Assuming that θ is small and sufficient signal to noise ratio, estimates of the data symbols $\hat{b}_I$ and

8

$\hat{b}_Q$ may be found using:

$$\hat{b}_I = \begin{cases} -1 & : & IdI < 0 \\ 1 & : & IdI \geq 0 \end{cases}, \qquad \hat{b}_Q = \begin{cases} -1 & : & QdQ < 0 \\ 1 & : & QdQ \geq 0 \end{cases}. \qquad [8]$$

5   In Figure 4, a discriminator 46 in series with the first I summing block 44A evaluates IdI and

outputs the estimate of the I data symbol $\hat{b}_I$ in accordance with equation [8]. This is a hard

decision. Similarly, another discriminator 46 in series with the first Q summing block 44C

evaluates the value of QdQ and outputs a hard-decision estimate of the Q data symbol $\hat{b}_Q$.

10   Using the estimates of equation [8], the cross terms may be removed from the cross-despread

values IdQ and QdI, by computing

$$IdQ_C = IdQ - \sum_{k=1}^{P_Q} \beta \alpha_I \hat{b}_I c_I c_Q \approx \sum_{k=1}^{P_Q} [\beta \alpha_I b_I c_I c_Q (\cos\theta - 1) + n_I c_Q] - \beta \alpha_Q b_Q P_Q \sin\theta \qquad [9]$$

$$QdI_C = QdI - \sum_{k=1}^{P_I} \beta \alpha_Q \hat{b}_Q c_Q c_I \approx \sum_{k=1}^{P_I} [\beta \alpha_Q b_Q c_Q c_I (\cos\theta - 1) + n_Q c_I] + \beta \alpha_I b_I P_I \sin\theta \qquad [10]$$

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where the subscript c is used to denote cross correlation (interference) has been substantially

removed. Equality in equations [9] and [10] is satisfied only if the data symbol estimates $\hat{b}_I$ and

$\hat{b}_Q$ are correct. This effectively reduces the interference terms by a factor of $(\cos\theta - 1)/\cos\theta$,

which is significant when θ is small. The area in which phase error is small is the area of greatest

20   interest, as the object is to continuously correct phase error and drive it as near as possible to zero.

For a continuously operating detector 32 operating on numerous data samples, any phase errors

that are initially large will be brought within a small error range in a relatively short time. Thus, a

phase error detector 32 must be precise in the area where θ is small.

9

In Figure 4, the second term to the right of the equality sign in equation [9], namely $\sum_{k=1}^{P_Q} \beta\alpha_I \hat{b}_I c_I c_Q$,

is achieved by multiplying the data estimate $\hat{b}_I$ from the discriminator 46 by the terms $\alpha_I\beta$ as in

equation [2] (which is known at the receiver), further multiplying by the spreading code $c_I(k)$ after

that code is delayed at a delay block 50A (to synchronize with its related data estimate with which

5   it is combined), and further multiplying that product ($\hat{b}_I \beta\alpha_I c_I$) by a cross spreading code c_Q,

similarly delayed at a delay block 50B. Figure 4 shows a series of three multipliers 48 used to

apply the interference term to the data estimate, though other functionally similar embodiments

may be used. These products are summed at a third I summing block 44E over all the P_Q chips

per symbol, then inverted (in sign) and input into an adder 52A. The other input to that same

10   adder 52A is the output of the second I summing block 44B, delayed at a third delay block 50C so

that the inputs married at the adder 52A correlate to the same symbol. The term IdQ in equation

[9] is the cross-despread value that is output from the second I summing block 44B. The term

$\sum_{k=1}^{P_Q} \beta\alpha_I \hat{b}_I c_I c_Q$ in equation [9] is the data estimate with interference that is inverted (in sign) and

input from the third I summing block 44E. The adder 52A combines the two terms as represented

15   in equation [9] and outputs the value IdQ_c, which is a despread value with interference from being

despread with the component spreading codes c_Q of the opposed signal component removed.

Processing on the $r_Q(k)$ signal component embodies the operation of equation [10], and mirrors

that done on the $r_I(k)$ signal component that embodies the operation of equation [9]. Similar

20   processing in parallel is shown in Figure 4. The output ($\sum_{k=1}^{P_I} \beta\alpha_Q \hat{b}_Q c_Q c_I$) of a third Q summing

block 44F is inverted (in sign) and added to the output (QdI) of the second Q summing block

44D. The result from adding these values at an adder 52B is the despread value QdI_c of equation

[10], which substantially lacks interference from being despread with the component spreading

codes c_I of the opposing signal component.

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When θ is sufficiently small, then equations [9] and [10] reduce to:

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$$IdQ_C \approx -\beta\alpha_Q b_Q P_Q \sin\theta + \sum_{k=1}^{P_Q} n_I c_Q \qquad [11]$$

$$QdI_C \approx +\beta\alpha_I b_I P_I \sin\theta + \sum_{k=1}^{P_I} n_Q c_I \qquad [12]$$

Due to the different component spreading codes $c_I(k)$ and $c_Q(k)$, these estimates are computed at different rates commensurate with the data rate difference illustrated in Figure 3. To compute values at the same rate, the receiver 26 preferably uses the estimated data symbols $\hat{b}_I$ and $\hat{b}_Q$ to remove the b_I and b_Q terms, at which point multiple samples may be accumulated in first-in/first-out registers of differing depths to normalize the streams to a common data rate. Since $b \in \{-1, 1\}$, then $b * \hat{b} = 1$. In particular, let $P_K = LCM(P_I, P_Q)$, wherein LCM(P_I, P_Q) represents the least common multiple of P_I and P_Q:

$$IdQ_A = \sum_{k=1}^{P_K/P_Q} IdQ_C \hat{b}_Q \approx -\beta\alpha_Q P_K \sin\theta + \sum_{k=1}^{P_K/P_Q}\left[\hat{b}_Q \sum_{k=1}^{P_Q} n_I c_Q \right] = k\alpha_Q \sin\theta + n_{IA} \qquad [13]$$

$$QdI_A = \sum_{k=1}^{P_K/P_I} QdI_C \hat{b}_I \approx +\beta\alpha_I P_K \sin\theta + \sum_{k=1}^{P_K/P_I}\left[\hat{b}_I \sum_{k=1}^{P_I} n_Q c_I \right] = k\alpha_I \sin\theta + n_{QA} \qquad [14]$$

Returning to Figure 4, the output IdQ_c of the adder 52A is multiplied by the data estimate $\hat{b}_Q$, which is taken from the opposing $r_Q(k)$ signal component, and delayed at a fourth delay block 50D to correlate symbols. The outputs of the related multiplier 54A are summed over all of the P_K/P_Q at a fourth I summing block 44G (that operates to perform $\sum_{k=1}^{P_K/P_Q} IdQ_c \hat{b}_Q$), which outputs IdQ_A as in equation [13] above. Similar processing occurs in parallel for the Q component of the signal $r_Q(k)$. Specifically, $\hat{b}_I$ from the opposing orthogonal signal component $r_I(k)$ is delayed at a

11

fifth delay block 50E and multiplied at a multiplier 54B with the output QdI$_C$ of the related adder

52B. A fourth Q summing block 44H (that operates to perform $\sum_{k=1}^{P_K/P_I} QdI_c \hat{b}_I$) sums over all of the

P$_K$/P$_I$ and outputs QdI$_A$ as in equation [14] above. Using P$_K$ drives the two signals IdQ$_A$ and QdI$_A$ to a common rate so that they may later be directly compared or combined.

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Since the two noise terms n_{IA} and n_{QA} of equations [13] and [14] are the accumulation of noise samples over the same length, and it is assumed that the original noise is circularly symmetric, then n_{IA} and n_{QA} have the same variance. Therefore, provided that the probability of decision errors is small on the I and Q samples, the relative quality of the estimates IdQ_A and QdI_A is

10   determined by the ratio of the scaling amounts α_I over α_Q. For example, when $\alpha_I > \alpha_Q$, then IdQ_A provides a better carrier phase loop detector signal.

In the preferred embodiment of Figure 4, both estimates are combined using a maximum ratio combining approach whereby the phase error detector 32 output may be computed using

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$$\hat{\theta}_e = \lambda_I QdI_A - \lambda_Q IdQ_A$$
$$= [\beta\lambda_I\alpha_I P_K + \beta\lambda_Q\alpha_Q P_K]\sin\theta$$
$$= \beta P_K[\lambda_I\alpha_I + \lambda_Q\alpha_Q]\sin\theta$$

where λ_I and λ_Q are scaling factors that are used to combine the individual estimates in order to maximize the signal to noise ratio of the estimate. The scaling factors λ_I and λ_Q are functions of

20   the scaling amounts α_I and α_Q. In Figure 4, the scaling factor λ_I is applied along the r$_Q$ signal component stream, and the scaling factor λ_Q is applied along the r$_I$ signal component stream. The products are then combined at an adder 52C (one input inverted in certain embodiments) to yield the estimate of the phase error $\hat{\theta}_e$, that is fed back in Figure 2 to the digital phase shifter 28 via the filter 36 and carrier loop 34.

12

The above approach may be streamlined (less hardware) by determining the estimate of the phase error $\hat{\theta}_e$ using only one or the other of the I and Q channels. Certain prior art circuits take such a one-channel approach by assuming (generally valid) that the stronger signal is on the Q channel,

$\left(\dfrac{E_b}{N_o}\right)_Q > \left(\dfrac{E_b}{N_0}\right)_I$, and so the prior art uses only the Q channel to estimate the phase error.

Mathematically, the prior art approach is $\hat{\theta}_e = sign(QdQ) \times IdQ$, where sign(QdQ) is from the set {-1, +1}. The present invention improves on the prior art in the one-channel approach by removing the cross correlation terms (subtracting the interference) from the I channel on the Q estimate, or vice versa. Mathematically, the one-channel embodiment of the present invention may be represented as either $\hat{\theta}_e = sign(IdI) \times QdI_c$ or $\hat{\theta}_e = sign(QdQ) \times IdQ_c$, wherein sign(QdQ) and sign(IdI) are from the set {-1, +1}. In Figure 4, the discriminator 46 outputs sign(IdI) by converting IdI to $\hat{b}_I$ (or outputs sign(QdQ) by converting QdQ to $\hat{b}_Q$), where $\hat{b}_I$ and $\hat{b}_Q$ are from the set {-1, +1} per equation [8]. Each of these one-channel approaches offer a more accurate estimate of the phase error as compared to the prior art, at the cost of increased complexity. Alternatively, the above one-channel phase error estimates may be scaled versions of the products shown, rather than the products directly. The preferred embodiment uses both of the above interference-corrected products, scaled to provide maximum signal to noise ratio SNR, and summed, to achieve a more stable $\hat{\theta}_e$ that reduces variance in the phase error detector 32, and consequently reduces jitter in the carrier loop 34.

The inventors have performed simulations on the one-channel embodiments of the present invention as compared to another of their inventions (co-pending) and to the prior art approach described above in the Background section. Figure 5 shows phase error estimates (phase error detector output) versus true phase angle error for the interference cancellation methods using IdQ_A and QdI_A , an approach of U.S. Patent Application No. XX/XXX,XXX, filed on January 22, 2004, assigned to the present assignee and hereinafter termed the DSRS CORDIC approach (Docket no. SL-164, 907A.0143), and the prior art approach which outputs the received I data

13

despread with the Q pn-code without interference cancellation. The results shown are for the case when $\alpha_I = 2$ and $\alpha_Q = 1$ corresponding to 6 dB more power on the I channel than on the Q channel, and for an overall SNR of 10 dB. All four of the S-curves in Figure 5 cross zero at zero degrees phase error, indicating that the different techniques will drive the carrier phase error to

5   zero. However, the resulting carrier loop phase jitter is a function of the variance of the samples used to compute the s-curves of Figure 5.

Figure 6 shows this variance as a function of the true phase angle error for each of the four different phase error detectors plotted in Figure 5. Figure 6 shows that the QdI_A and the DSRS

10   CORDIC approach, have nearly identical variance. The IdQ_A has approximately 6 dB higher variance, a result of the fact that there is 6 dB less power in the Q signal than in the I signal. Finally, when compared to the prior art approach of using IdQ, the variance of QdI_A is nearly 20 dB lower in the region from –45 to 45 degrees (the region of most interest). Therefore, one would expect that either the DSRS CORDIC approach or the QdI_A will result in lower untracked phase

15   noise at the carrier loop output and hence improved performance.

Relative to the DSRS CORDIC approach, using either IdQ_A or QdI_A (depending on which signal provides the better error signal) requires less complex hardware. The present invention requires despreading, spreading and subtraction whereas the DSRS CORDIC approach requires

20   despreading, spreading, subtraction, and the implementation of a CORDIC.

While there has been illustrated and described what is at present considered to be a preferred embodiment of the claimed invention, it will be appreciated that numerous changes and modifications are likely to occur to those skilled in the art. It is intended in the appended claims

25   to cover all those changes and modifications that fall within the spirit and scope of the claimed invention.

14